(19) JAPANESE PATENT OFFICE (JP)

(12) Publication of Unexamined Patent Application (A)

(11) Japanese Patent Application Disclosure No.: H3–91239

(43) Disclosure Date: April 16, 1991

(51) Int. Cl.[5]	Identification Code	JPO File No.
H 01 L 21/28	301 A	7738-5F
21/205		7739-5F
21/285	C	7738-5F

Request for Examination: Not requested Number of Claims: 4 (7 pages total)

---

(54) Title of the Invention: Thin Film Formation Method

(21) Application Number: H1–227351

(22) Filing Date: September 4, 1989

(72) Inventor: Takashi Kobayashi
c/o Hitachi Ltd. Central Research Laboratories
1-280 Higashi Koigafuchi, Kokubunji-shi, Tokyo

(72) Inventor: Atsushi Hiraiwa
c/o Hitachi Ltd. Central Research Laboratories
1-280 Higashi Koigafuchi, Kokubunji-shi, Tokyo

(72) Inventor: Shinpei Iijima
c/o Hitachi Ltd. Central Research Laboratories
1-280 Higashi Koigafuchi, Kokubunji-shi, Tokyo

(71) Applicant: Hitachi Limited
4-6 Kanda, Surugadai, Chiyoda-ku, Tokyo

(74) Agent: Katsuo Ogawa, Patent Attorney (and one other)

Specifications

1. Title of the Invention

Thin Film Formation Method

2. Scope of Patent Claims

1. A thin film formation method whereby a silicon film is formed on a substrate having a desired stepping, while impurity doping is performed using a low-pressure chemical vapor deposition method, said method characterized by the fact that blended gas containing disilane or trisilane and arsine is used as the source gas.

2. A thin film formation method according to Claim 1, characterized by the fact that the formation of said silicon film is performed at 450°C or above and 550°C or below.

3. A polycrystalline silicon film formed by the thin film formation method of Claim 1 or 2, wherein when subsequent polycrystallization by heat treatment is performed, crystal grains are contained having a granule diameter at least 10 times that of the film thickness, and the surface roughness is no greater than 5 nm.

4. Semiconductor device which is provided with a polycrystalline silicon film specified in Claim 3 and contains arsenic.

3. Detailed Description of the Invention

(Industrial Field of Application)

The present invention relates to a thin film formation method, more specifically, method of realizing lower resistance of wiring in the steep stepped portions and reduction of impurity diffusion into the substrate, simplifying the manufacture of LSI devices, and the formation of a silicon film containing suitable amounts of arsenic for temperature reduction.

(Prior Art)

Polycrystalline silicon (Si) films, which are formed by a low-pressure chemical vapor deposition method (LPCVD method) using the thermal decomposition of monosilane (SiH_4), are widely used in electrodes or wiring for semiconductor devices. Since polycrystalline Si films formed

by LPCVD method, when used alone, have an extremely high resistance, in subsequent processing, impurities are introduced by means of a commonly known thermal diffusion method or ion implantation method, and conductivity is obtained. Matters relating to these kinds of thin film formation methods are discussed in, for example, Journal of the Electrochemical Society, 127 (1980) pp. 686-690.

(Problems That the Invention Is to Solve)

In the prior art described above, when ion implantation is performed in a polycrystalline silicon film, in the steep stepped sidewall portion, areas are produced where the impurity concentration is insufficient, and it is not possible to provide sufficient conductivity for electrodes or wiring. Further, in order to diffuse and activate the implanted impurity, a heating treatment of at least 900°C has been necessary.

On the other hand, in doping of impurities by thermal diffusion method, if diffusion is performed at a high temperature and for a long period of time, doping of the steep stepped sidewall portions is possible. However, in the areas where the polycrystalline silicon film comes into contact with the silicon substrate, impurities are diffused into the substrate, creating the problem of disturbance of impurity distribution in the source and drain areas which constitute a MOS transistor, for example.

Furthermore, in capacitors having a groove structure, when an electrode that has been imbedded in the groove is formed of polycrystalline silicon, and an ion implantation method or heat diffusion method has been performed, it has been difficult to achieve doping of a sufficient quantity of impurities into the polycrystalline silicon as a whole.

One method of solving the problems described above has been a method whereby the polycrystalline silicon film is formed while impurity doping is performed (*in situ* doping method). Specifically, this is a method whereby, together with the SiH_4, the impurity source of phosphine (PH_3), diborane (B_2H_6), arsine (AsH_3), or the like is made to flow simultaneously, and impurity doping is performed while the polycrystalline silicon film is formed. However, in the case of film formation using SiH_4 and PH_3 or AsH_3, there have been problems such as the fact that the growth rate is reduced by as much as one figure in comparison with instances where PH_3 or AsH_3 is not added, reducing productivity, and the fact that, since a heating treatment at high temperature of 900°C to 1000°C has been required in order to sufficiently activate the impurity, and it has not been

possible to avoid the diffusion of the impurity into the substrate silicon, as in the thermal diffusion method.

In order to increase the film deposition rate, a method has been attempted whereby Si_2H_6 is used instead of SiH_4. However, in techniques used up to now, even if Si_2H_6 and PH_3 are used as the source gases, a heating treatment of 900 to 1000°C is necessary to activate the impurities. Moreover, since phosphorus has a greater dispersion constant than arsenic, so long has PH_3 is used as the source gas, diffusion of the impurity into the substrate silicon cannot be avoided.

The object of the present invention is to offer a thin film forming method wherein the problems in Prior Art described above are solved, and a silicon film having high conductivity can be formed with excellent productivity and hardly any impurity diffusion into the substrate silicon.

(Means Used to Solve the Problems)

The aforesaid object is achieved by the following:

(1) Using a mixed gas containing Si_2H_6 or Si_3H_8 (trisilane) and AsH_3 as the source gas.

(2) Making the film formation temperature at least 450°C and no higher than 550°C.

(Operation)

In gas phase, Si_2H_6 decomposes as:

$$Si_2H_6\ (g) \rightarrow SiH_2\ (g) + SiH_4\ (g)$$

producing SiH_2 (silylene).

Since SiH_2 has a higher reactivity than SiH_4, adsorption into the substrate silicon surface by AsH_3 is not blocked. Accordingly, the film can be deposited at high rate whether or not AsH_3 is present.

When Si_2H_6 and AsH_3 are used as the source gas, a film formed at a formation temperature of 550°C or below is amorphous. This film is crystallized by heat treatment at a comparatively low temperature of 650°C for 15 minutes, but thereafter changes in the crystal grain size are not produced even when heat treatment is performed at a higher temperature. Moreover, the arsenic that has been introduced as the impurity is completely activated by heat treatment at 650°C. Thus, sufficient conductivity can be obtained at heat treatment of 650°C, and no changes in resistivity will be created even if he treatment is performed at a higher temperature.

It is public knowledge that, when arsenic ions are implanted in a silicon film in a

polycrystalline state, and when a polycrystalline silicon film is formed while arsenic doping is performed, the crystal grains cannot grow unless heat treatment is performed at 900°C or above.

As explained above, when an amorphous silicon film is formed while doping with arsenic is performed by using Si_2H_6 and AsH_3 as source gases, activation of the impurity in the film and growth of the crystal grains are completed by heat treatment at about 650°C. For this reason, even if high temperature heat treatment is not performed as in previous methods, a silicon film containing arsenic with a sufficiently low resistance is obtained. Moreover, arsenic has a diffusion coefficient in silicon on an order one figure less than that of phosphorus. Accordingly, by means of the present invention, it is possible to prevent the diffusion of impurities into the silicon layer below.

(Examples of Embodiment)

Working examples of the present invention are explained below.

Working Example 1

Figure 3 is a schematic drawing showing the device used in tests. A jig 30 was placed in the center of a quartz tube 10, and sample substrates 40 or placed therein at intervals of 18 mm. The sample substrates used were formed by forming a 100 nm thermal oxidation film on silicon.

After the mounting of the substrates 40 and the evacuation of the quartz tube 10, a valve 50 and valve 60 were opened, and 50 cc/min of Si_2H_6 and 0.2 cc/min of AsH_3 were introduced simultaneously. The internal pressure of the quartz tube 10 while the Si_2H_6 and AsH_3 were introduced was maintained at 30 Pa. After film deposition was induced by introduction of the gases for a specified period of time, the sample substrates 40 were removed. Next, heat treatment was performed for 20 minutes in a nitrogen atmosphere at 650°C, 800°C, 900°C, and 1000°C. The heat-treated samples were measured for resistivity by 4-probe method, and for carrier concentration and mobility by hole effect measurement.

Figure 1 shows the measurement results for resistivity in the aforesaid substrates 40. The horizontal axis shows the heat treatment temperature and vertical axis the resistivity of the films. Here, the effects obtained when the film formation temperatures were made 525°C, 550°C, and 575°C are shown. When the film formation temperature was higher than 550°C, the resistivity decreased in accordance with the increase in the heat treatment temperature. In contrast, when the film formation temperature was 550°C or below, sufficient conductivity was obtained with heat treatment at 650°C, and no changes in the resistivity occurred even after heat treatment at higher

temperature. Moreover, films formed at a temperature of 550°C or below were amorphous, retaining their state when formed.

Figure 2 shows measurement results for the carrier concentration with regard to the aforesaid substrates 40, indicating the heat treatment temperature in the horizontal axis and the carrier concentration in the vertical axis. As with resistivity, a film formation temperature of 550°C or below, the carrier concentration remained roughly constant regardless of the heat treatment temperature.

From Figure 1 and Figure 2 it can be seen that silicon films which have been formed at 550°C or below while being doped with arsenic exhibit no change in electrical characteristics after activation of the impurity by heat treatment at 650°C, no matter at how high a temperature subsequent heat treatment is performed.

Figure 1 and Figure 2 also show results obtained by conventional methods for purposes of comparison. Here the conventional method is one whereby SiH_4 and AsH_3 were used as the source gas, SiH_4 was introduced at 200 cc/min and AsH_3 at 0.2 cc/min under the conditions of 630°C and 80 Pa, and the silicon film was formed while arsenic doping with performed. This film was polycrystalline, retaining its state when formed. Although similar treatment was performed as when Si_2H_6 and AsH_3 were used, heat treatment at a temperature of 900°C or higher was necessary in order to activate the impurity.

It is a publicly known fact that, when a 200 nm silicon film in a polycrystalline state is formed at 630°C using SiH_4 and arsenic ions implantation is performed thereon, heat treatment of the least 900°C is necessary in order to activate the impurity.

In accordance with this Example of Embodiment, by forming the silicon film at 550°C or below while performing arsenic doping, using Si_2H_6 and AsH_3 as the source gases, it was possible to activate the impurity by heat treatment at a much lower temperature (approximately 650°C) than when a polycrystalline silicon film was formed while arsenic doping was performed using Si_2H_4 and AsH_3 as source gases, or when doping of arsenic with performed by ion implantation into a polycrystalline silicon film. Moreover, there was the additional advantage that the resistivity of the film did not change even when the heat treatment temperature subsequent to film formation was varied.

In films having a film formation temperature of 550°C or below, the carrier mobility is at least 40 $cm^2/v \cdot s$, approximately twice that obtained by conventional methods. From observation by transmission-type electron microscope, it was clear that films formed at 550°C or below contain crystal granules of the least 10 times the silicon film formed by conventional methods, i.e., approximately 10 times the film thickness. Accordingly, as shown in Figure 1 and Figure 2, it is possible to obtain sufficient conductivity even with a lower impurity concentration than in the past. For this reason, there is also the effect of being able to reduce the amount of impurity diffusion into the base silicon substrate.

Working Example 2

This Example of Embodiment shows instances where it can be determined to what extent the wiring resistance differs according to the method of impurity introduction, when a polycrystalline silicon film is used in wiring on a steep stepped part.

In the procedure shown in Figure 4, Sample A and Sample B were prepared. First, a thermal oxidation film 102 having a thickness of 1 μm was formed on the silicon substrate 101 (Figure 4 (a)). Next, using publicly known lithography and dry etching techniques, grooves 103 having a width of 0.8 μm were formed at equal intervals (Figure 4 (b)). Next, a SiO_2 film 104 was formed to 100 nm by LPCVD process (Figure 4 (c)).

Next, silicon film formation and impurity doping were performed by the following method.

With Sample A, a 200 nm polycrystalline silicon film was formed while arsenic doping was performed by simultaneously introducing 50 cc/min of Si_2H_6 and 0.2 cc/min of AsH_3 into a quartz tube having an internal temperature 525°C at a pressure of 30 Pa.

With regard to Sample B, a 200 nm polycrystalline silicon film was formed using SiH_4 as a source gas inside a quartz tube at 630°C and 80 Pa, then arsenic ions were implanted in the amount of $5 \times 10^{15} cm^{-2}$ at an implantation energy of 180 KeV.

Next, Sample A and Sample B were each subjected to 60 minutes of heat treatment at 650°C and 900°C, respectively.

The sheet resistance in the flat portions of the silicon film of Sample A was 50 Ω/□, and resistance of the wiring having a width of 0.8 μm traversing 10 steps was 3.0 KΩ, indicating that sufficient conductivity was obtained. In Sample B, sheet resistance in the flat portions of the silicon film was 120 Ω/□, and resistance of the wiring having a width of 0.8 μm traversing 10 steps was

extremely high at 350 KΩ.

This Example of Embodiment, by forming a silicon film while performing doping with arsenic, thus offers the effect of providing a much lower wiring resistance in the steep stepped portions than in conventional ion implantation methods.

Working Example 3

This Example of Embodiment illustrates an instance where the effect of differences in the impurity doping method on impurity diffusion depth into the substrate silicon was measured.

The substrate shown in Figure 4 (b) was used as a sample. Using the device shown in Figure 3, Sample C was prepared by forming a 200 nm silicon film containing arsenic on the sample substrate 40 while simultaneously introducing 50 cc/min of Si_2H_6 and 0.2 cc/min of AsH_3 into a quartz tube having an internal temperature 525°C at a pressure of 30 Pa. Next, heat treatment was performed at 650°C for 60 minutes in a nitrogen atmosphere.

Sample D was produced by forming a 200 nm polycrystalline silicon film in a quartz tube at a temperature of 630°C and a pressure of 80 Pa using SiH_4 as a source gas. Next, arsenic ion implantation with performed in the amount of $5 \times 10^{15}cm^{-2}$ at an implantation energy of 180 KeV, and then heat treatment was performed for 60 minutes in a nitrogen atmosphere at 900°C.

After heat treatment, Sample C and Sample D were cleaved along a plane perpendicular to the grooves 103, etched with a blended solution of hydrofluoric acid and nitric acid, the cross sections were examined by scanning electron microscope, and evaluated using the diffusion layer width x in Figure 4 (d) as the diffusion depth.

While the diffusion depth in Sample D was 0.1 μm, the diffusion depth in Sample C was so slight as to be negligible, at 0.01 μm or less,

This Example of Embodiment offers the effect that, by using Si_2H_6 and AsH_3 as source gases and forming the silicon film in an amorphous state while doping with arsenic, the heat treatment for activation can be performed at a much lower temperature, so that the impurity diffusion depth into the substrate is so slight as to be negligible.

Working Example 4

In this Example of Embodiment, the relation between the silicon film formation method and the surface roughness of the film was measured.

The surface roughness of the silicon films in Samples C and D, the cross sections of which were examined by scanning electron microscope in Working Example 3, was examined by scanning electron microscope.

In this Example of Embodiment, the surface of the silicon film formed in an amorphous state (Sample C) by using Si_2H_6 and AsH_3, at 525°C, was completely smooth, with absolutely no roughness observed at a magnification factor of 50,000. In contrast, surface roughness of approximately 0.1 μm was observed on the surface of Sample D, where arsenic ion implantation was performed after the formation of a polycrystalline silicon film as a comparative example. In addition, the surface conditions of Sample C and Sample D did not change even after heat treatment was performed.

In Sample 3, the silicon film was formed at 525°C, but if the film formation temperature is 575°C or below, a smooth surface can be obtained. On the surface of a polycrystalline silicon film formed while adding arsenic at 630°C, using SiH_4 instead of Si_2H_6 as a source gas, fine irregularities of about 0.05 μm were observed.

This Example of Embodiment offers the effect that an extremely smooth silicon surface can be obtained by forming the silicon film in an amorphous state while doping with arsenic is performed using Si_2H_6 and AsH_3 as source gases.

Working Example 5

This Example of Embodiment shows an instance where the present invention is used in the formation of a MOS type transistor.

The sample prepared is shown in Figure 5. First, a field oxidation film 202 was formed by a publicly known selective oxidation technique on the surface of a 10 Ω · cm (100) p-type silicon substrate 201. Next, the silicon substrate was oxidized in an oxygen atmosphere, forming a 20 nm gate oxidation film 203. Next, after a 200 nm polycrystalline silicon film 204 was formed by LPCVD method, thermal diffusion of phosphorus with performed, and a gate electrode was formed by the processing thereof. Next, after phosphorus and arsenic ion implantation were performed in sequence, heat treatment was performed for 60 minutes in a nitrogen atmosphere at 900°C, and a source-drain region 205 was formed. Next, an inter-layer SiO_2 film 206 was formed by CVD method.

Next, 50 cc/min of Si_2H_6 and 0.2 cc/min of AsH_3 were introduced into a quartz tube having an internal temperature 525°C at a pressure of 30 Pa, and a 200 nm silicon film 207 was formed in

an amorphous state while arsenic doping was performed. Heating treatment was then performed for 60 minutes at 650°C in a nitrogen atmosphere, and the crystallization of the silicon film and activation of the arsenic were induced. The silicon film 207 was then processed to form draw-out wiring.

For purposes of comparison, as a conventional technique, a silicon film 207 was formed in a polycrystalline state, subjected to arsenic ion implantation under the conditions of 180 KeV and $5 \times 10^{15}cm^{-2}$, then heat treatment was performed at 900°C in a nitrogen atmosphere for 60 minutes, and a sample was obtained on which draw-out wiring was formed.

The MOS-type transistor produced by the method of present invention had a lower wiring resistance and higher punch-through voltage resistance than that produced by the conventional method.

By means of the present invention, by using a silicon film which has been formed in amorphous state using Si_2H_6 and AsH_3 while performing arsenic doping, and then crystallized, as the draw-out wiring of a source-drain of a MOS type transistor, the on-through voltage resistance of the transistor can be increased.

In Working Example 1 through Working Example 5 described above, tests were performed under limited conditions. When the temperature of the quartz tube was lower than 450°C, the film growth rate was greatly reduced under 1 nm/min, markedly decreasing throughput, which is suitable for the manufacture of actual LSI devices. When the temperature in the quartz tube is higher than 550°C, as shown in Figure 1 or Figure 2, the resistivity and carrier concentration and mobility of the film greatly change according to the heat treatment temperature, so controllability is poor. If the internal temperature of the quartz tube is within a range of 450°C or above and 550°C or below, the desirable effects in each of the examples of embodiment can be obtained. Moreover, even when Si_3H_8 is used instead of Si_2H_6, the desirable effects of each of the examples of embodiment can be obtained. Additionally, by blending inert gases such as nitrogen and helium as a carrier gas, the uniformity of film thickness and resistance among wafers can be increased. Needless to say, the present invention is effective in these cases as well.

(Effects of the Invention)

By means of the present invention, it is possible to form a silicon film containing arsenic and

having the desired impurity distribution in the film thickness direction. The impurity in this silicon film can be activated by heat treatment at a much lower temperature than in conventional methods. Accordingly, the impurity is not uncontrollably diffused into the substrate, and it becomes possible to dope a polycrystalline silicon on steeply stepped side walls or inner grooves, achieving a reduced resistance in electrode and wiring. Furthermore, in the manufacture of LSI devices, processing can be greatly simplified and temperature reduction achieved, adding the effect of increasing yield and reducing production costs.

4. Brief Explanation of the Drawings

Figure 1 is a measurement graph showing the correlation between heat treatment temperature and resistivity in silicon in films produced according to a Example of Embodiment of present invention and a comparative example, Figure 2 is a measurement graph showing the correlation between the heat treatment temperature and carrier concentration in silicon thin films produced according to a Example of Embodiment of the present invention and a comparative example, Figure 3 is a schematic lateral cross-sectional view of a device used in implementing the present invention, Figure 4 is a cross-sectional diagram showing the sequence of producing samples used in examples of embodiment of the present invention, and Figure 5 is a cross-sectional view of a semiconductor device prepared using the method of the present invention.

10... quartz tube, 20... heater, 30... jig, 40... substrate, 50, 60, 70... valve, 80... exhaust system, 101... silicon substrate, 102... thermal oxidation film, 103... stepped portion, 104... CVD SiO_2 film, 105... polycrystalline silicon film, 106... diffusion layer, 201... silicon substrate, 202... field oxidation film, 203... gate oxidation film, 204... phosphorus-doped silicon film, 205... diffusion layer, 206... CVD SiO_2 film, 207... arsenic-doped silicon film.

Agent: Katsuo Ogawa, patent attorney [seal]

Figure 1

[see source for figure]

[vertical axis] Resistivity (Ω·cm)

[horizontal axis] Heat treatment temperature (°C)

[in graph] Conventional method

Film formation temperature

Figure 2

[see source for figure]

[vertical axis] Carrier concentration (cm^{-3})

[horizontal axis] Heat treatment temperature (°C)

[in graph] Film formation temperature

Conventional method

Figure 3

[see source for figure]

Figure 4

[see source for figure]

Figure 5

[see source for figure]